

Organic Field Effect Transistors for Large Format Electronics

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Final Report

**Technical Monitor: Latika Becker
MDA**

**Submitted by
Dr. Andrew Wowchak
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**SVT Associates, Inc.
7620 Executive Drive, Eden Prairie, MN 55344**

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1. Summary of Project Results

The work performed for this program was carried out at SVT Associates and the University of Minnesota. We have succeeded in demonstrating an Organic Field Effect Transistor (OFET). We investigated a bottom-contact transistor structure in which the source and drain contacts are deposited directly on the gate oxide followed by the deposition of the active organic layer. Two-dimensional simulations for these structures were carried out and the I-V characteristics calculated. Barrier lowering due to image charge effects was found to play a critical role in determining device characteristics because the source contact acts as a reverse biased Schottky contact and without this effect the drain current would be severely limited. One important consequence of this is that if material in the immediate vicinity of the contacts is depleted of carriers due to traps or other defects the current can be significantly reduced. Even though this layer may constitute as little as 1% of the channel material, device performance is disproportionately affected by it. Actual bottom-contact OFET devices were fabricated and tested. Various organic materials were deposited onto the contact/oxide layer. We have obtained device I-V curves with characteristic transistor behavior similar to the modeling result. It was found that ultraviolet light can greatly enhance current magnitude. These results represent significant accomplishments toward achieving our Phase I program goals. In summary, the major results of this Phase I program are:

- ❖ **Development of two-dimensional model showing importance of:**
 - **image charge related barrier lowering on current magnitude**
 - **material quality in the immediate vicinity of the source/drain contacts**
- ❖ **Fabricated and tested OFETs with various organic materials**
- ❖ **Demonstrated working OFETs with channel lengths of 10, 20 and 30 μm**

2. Introduction

Essentially all of today's microelectronic devices are made from inorganic materials – silicon and gallium arsenide being principal among them. Recently, devices made from organic molecules have been gaining attention. Although still in the early stages of development significant progress has been achieved. One of their key distinguishing features is compatibility with flexible substrates (see Figure 1) which makes them amenable to applications not possible with their inorganic counterparts. They also have the potential for low-cost and low-temperature processing making them attractive for the commercial market. Organic light emitting diodes (OLED's) are already in production by various manufacturers as an alternative technology for displays in cell phones and PDA's, but the electrical properties of organic compounds have not been as well exploited due to technical difficulties. By developing the OFET one can envision the enabling of large area display drivers (together with organic light emitters), and electronic circuits on smart cards, just to name a couple applications that could be widely used for the military.

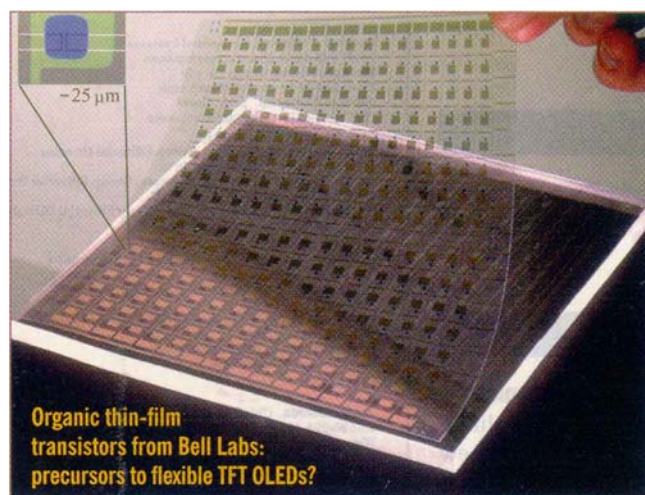


Figure 1. Organic devices fabricated on a flexible substrates (EE Times, January 6, 2003).

Generally organic molecules or polymers are plastic-like materials distinguished by excellent mechanical properties such as strength and flexibility and not by their electrical properties such as conductivity. Some of these materials, commonly called “conjugated”, can be made into semiconductors or even electrical conductors. There still remain significant differences between organic and inorganic materials. In particular, organic materials are bound together by weak van der Waals force rather than the covalent or ionic bonds in inorganic materials. This makes it more difficult for charge carriers to move from molecule to molecule, but room temperature mobilities high enough to make organic field effect transistors (OFETs) practical have already been observed. Although these mobilities are somewhat higher than the mobilities achieved in amorphous silicon they still remain quite a bit less than that of poly- or single-crystalline silicon where mobilities can reach values of several hundred $\text{cm}^2/\text{V}\cdot\text{s}$. The switching speed of OFETs is limited by the weak nature of the van der Waals force and this, in turn, will ultimately determine what types of applications are suitable for these devices. Nonetheless, if OFETs can be successfully developed many new technologies will become possible.

For the Phase I program our efforts were concentrated on the bottom-contact structure depicted in Figure 2. The source and drain contacts are formed directly on the gate insulator. The organic active layer is subsequently deposited to cover the source/drain contacts and the gap between them. This type of structure is less dependent on the physical restrictions imposed by the nature of the organic material than the top contact types of structures which require the deposition of contacts directly onto the organic layer. For the latter high temperature processing steps are not feasible and requires the use of shadow masks which have limited resolution (\sim few μm). The bottom-contact structure, on the other hand, can take full advantage of high resolution lithography tools for defining the contacts and channel lengths.

The OFETs resemble conventional thin film transistors. There is one significant difference between them and devices made from inorganic compounds. Since organic crystals are bonded by van der Waals forces, it is not necessary for them to be lattice-matched to the substrate on which they are grown. Therefore they can be deposited quasi-epitaxially to form an ordered, relatively dislocation-free film on a variety of substrates.

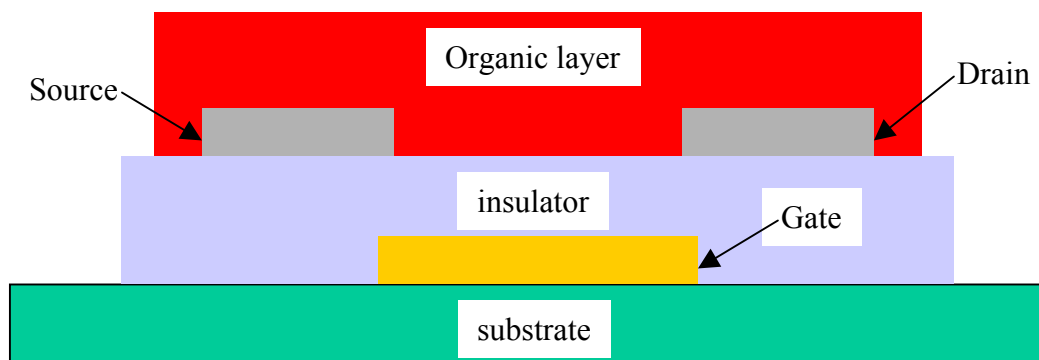


Figure 2. Diagram of a bottom-contact organic field effect transistor (OFET).

3. Modeling Results

As in conventional thin film transistors, in an OFET the conducting channel forms in the organic material at the interface to the gate insulator. The polymer is usually not doped and hence, the charge carriers forming the conducting channel need to be injected from the contacts. This poses significant challenges for the fabrication of low resistance paths between the metal source and drain electrodes and the induced channel. In normal operation, the gate voltage is used to induce a channel of variable charge carrier density between source and drain. Thus the gate voltage controls the source/drain current.

Professor Paul Ruden at the University of Minnesota has developed a two-dimensional device model that correctly describes the injection and extraction processes (including self-consistent barrier lowering due to image charge effects). This barrier lowering effect is crucial, because the injecting source contact is essentially a reverse biased Schottky contact and, in the absence of the barrier lowering effect, the drain current would be severely limited by the contact. An illustrative result is shown in Figure 3, where calculated output characteristics for a p-channel

pentacene OFET with $2\mu\text{m}$ source to drain spacing are plotted. (The current is normalized to the gate width; a $100\mu\text{m}$ wide device of this channel length would support drain currents of hundreds of μA). The data demonstrates the large effect that the image charge-induced barrier lowering has on the device performance. This is only one of the phenomena associated with the source and drain contacts that are of critical importance to the development of OFETs in order to be competitive with more conventional transistors.

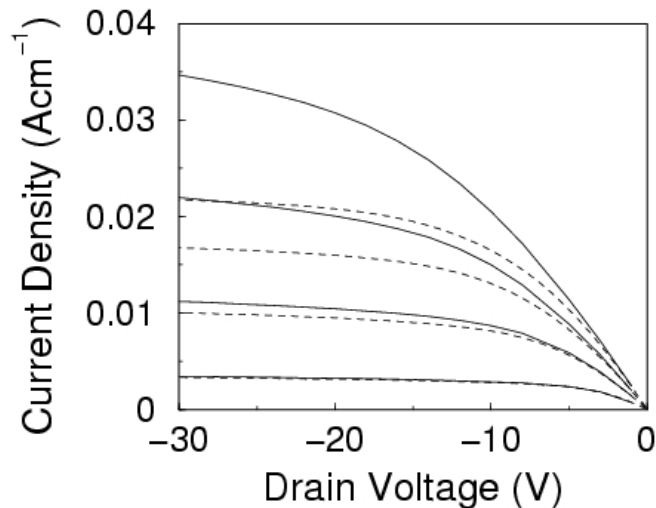


Figure 3. Calculated output characteristics of a pentacene OFET with image charge induced contact barrier lowering (solid) and without that effect (dashed). Current out of the drain terminal is counted as positive. The gate-to-source voltages for the different I_d vs. V_{ds} curves are -5V , -10V , -15V , and -20V .

As a second example, a polyhexylthiophene (P3HT) OFET is examined. The source to drain contact spacing (channel length) for this device is taken to be $5\mu\text{m}$. Figures 4 and 5 show the calculated output characteristics. Because of the lower field effect mobility of this material system and the somewhat larger channel length, the output current of the device is considerably smaller. (An actual device of $100\mu\text{m}$ width would yield currents in the hundred nA range).

Channel Contact Formation

Contacts of bottom-contact OFETs are typically of the general shape shown in Figure 6. Ideally, the charge carriers are injected and extracted from the channel over a thickness d_{ch} , corresponding to the effective thickness of the channel, along the vertical face of the contact. Since d_{ch} is only on the order of $1 - 2\text{nm}$, this ideal situation is approached only if the organic material deposited in the immediate vicinity of the metal is of high quality, i.e., that it does not contain many traps, grain boundaries, or even voids. However, if this is not the case, contact to the channel is still made, but, because the charge carrier concentration in the undoped organic material decreases rapidly with increasing distance from the gate insulator, the resultant contact resistance is large. Clearly, the quality of the contact depends sensitively on the organic material deposition process and on the shape and dimensions of the metal contact. The metal may partially block deposition next to the vertical sidewall due to shadowing, or it may influence the

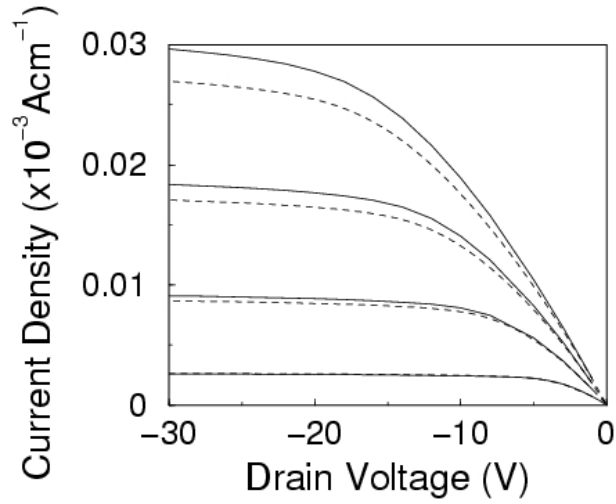


Figure 4. Calculated output characteristics of a P3HT OFET with image charge induced contact barrier lowering (solid) and without that effect (dashed). The zero-field barrier height is 0.3eV. Current out of the drain terminal is counted as positive. The gate-to-source voltages for the different I_d vs. V_{ds} curves are -5V, -10V, -15V, and -20V.

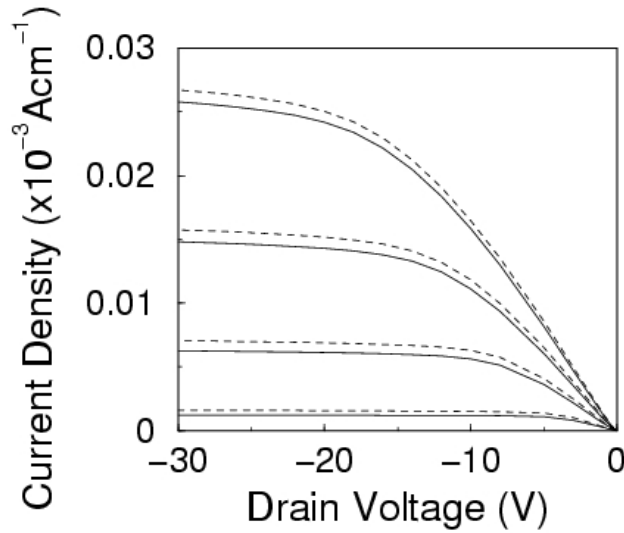


Figure 5. Calculated output characteristics of a P3HT OFET with two different injection models, corresponding to infinite (dashed) and finite (solid) recombination velocity. The zero-field barrier height is 0.5eV. Current out of the drain terminal is counted as positive. The gate-to-source voltages for the different I_d vs. V_{ds} curves are -5V, -10V, -15V, and -20V.

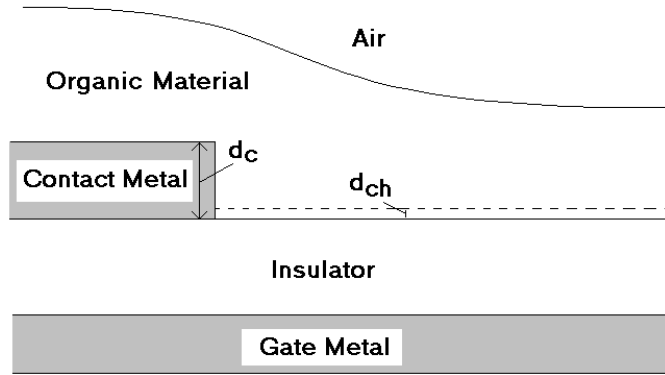


Figure 6. Cross section view of a part of an OFET in the vicinity of a source or drain contact.

local ordering due to surface energy effects. The development of optimized contact formation in OFETs is critical because of the large influence that these contacts have on device performance.

To simulate the consequences of defects in the material adjacent to the contacts, appropriate calculations were done. Representative results in terms of output characteristics are shown in Figure 7. Here two different contact barrier heights are examined: 0.0eV (dashed) and 0.3eV (solid). The latter case may be compared with the results plotted in Figure 4. The calculations show that the current is reduced by about 25% if the small region in the immediate vicinity (less than 1% of the channel length) is depleted of carriers due to traps or simply has a very low

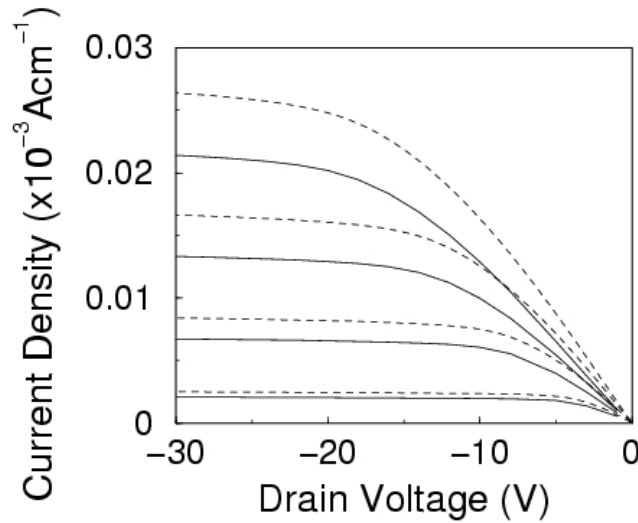


Figure 7. Calculated output characteristics of P3HT OFETs with highly disordered contact regions and two different (zero-field) contact barrier heights: 0.0eV (dashed) and 0.3eV (solid). Current out of the drain terminal is counted as positive. The gate-to-source voltages for the different I_d vs. V_{ds} curves are $-5V$, $-10V$, $-15V$, and $-20V$.

mobility. The astonishingly strong effect, given the small fraction of the material volume affected, arises because the charge carriers under these circumstances enter the channel after being injected into the organic material from the top surface of the contact where the barrier lowering electric field is much reduced relative to the vertical face. This type of result indicates that the material deposition in the immediate vicinity of the contacts is critical for achieving good device performance.

The contact related effects are currently being investigated further by modeling transient effects. Clearly, it may be expected that the speed of an OFET will be impacted by the contacts. The injection process described above will limit the speed with which the charge in the channel may be varied by changes in the gate bias. Very roughly one may model the delay time for this type of channel modulation as:

$$\tau = \tau_{\text{channel}} + \tau_{\text{contact}}$$

The modeling done indicates that under ideal conditions τ_{contact} is comparable to τ_{channel} . However, even relatively small regions of highly disordered organic material in the immediate contact vicinity may yield $\tau_{\text{contact}} \gg \tau_{\text{channel}}$, causing a significant loss in device speed.

To summarize, two-dimensional simulations of the characteristics of bottom contact OFETs demonstrate that the material in the immediate vicinity of the contacts is of critical importance. Even though this material may constitute only a small fraction of the channel material, near ideal current and speed performance is disproportionately affected by it. Importantly, the modeling provides a guideline for the expected device behavior so we can compare with actual device measurement.

4. OFET Fabrication

The basic structure of an organic transistor (OFET) is very similar to that of the traditional metal oxide semiconductor field effect transistor or MOSFET that is the workhorse of silicon technologies. When a negative voltage is applied to the gate an accumulation layer of holes forms at the interface between the organic semiconductor and the insulator layers so that current can flow between the source and drain contacts. The structure is the bottom-contact one described in the preceding section.

For the gate and gate oxide we used pieces cut from 4" p-type silicon wafers that had a 2500 Å layer of thermally grown oxide. The wafers were 500 – 550 µm thick with resistivities in the range of 1 – 10 Ω-cm. The gate contact was formed by depositing a thin Ti layer followed by a gold layer onto the backside of the silicon wafer. The Ti layer was required since gold does not adhere well to silicon.

Gold source and drain contacts were subsequently patterned and deposited onto the SiO₂ using standard lithography and lift-off techniques. A thin layer of Ti was again used to promote better contact. These contacts are essentially adjacent metal bars 50, 100, 150 or 250 µm in length and 750 µm wide. Their separation which defines the transistor channel length varies from 10 to 70 µm in 10 µm steps.

To complete the OFET structure a thin layer of organic material is deposited directly on top of the oxide and the source/drain contacts. Figure 8 shows a detailed view of the OFET structure including nominal dimensions. One of the important physical characteristics of this device is how well the organic material covers the vertical features defined by the source/drain contacts. As suggested by the modeling the nature of the metal/organic interface is a key factor in determining overall device performance. The presence of voids or other material faults at the interface will lead to greatly degraded performance.

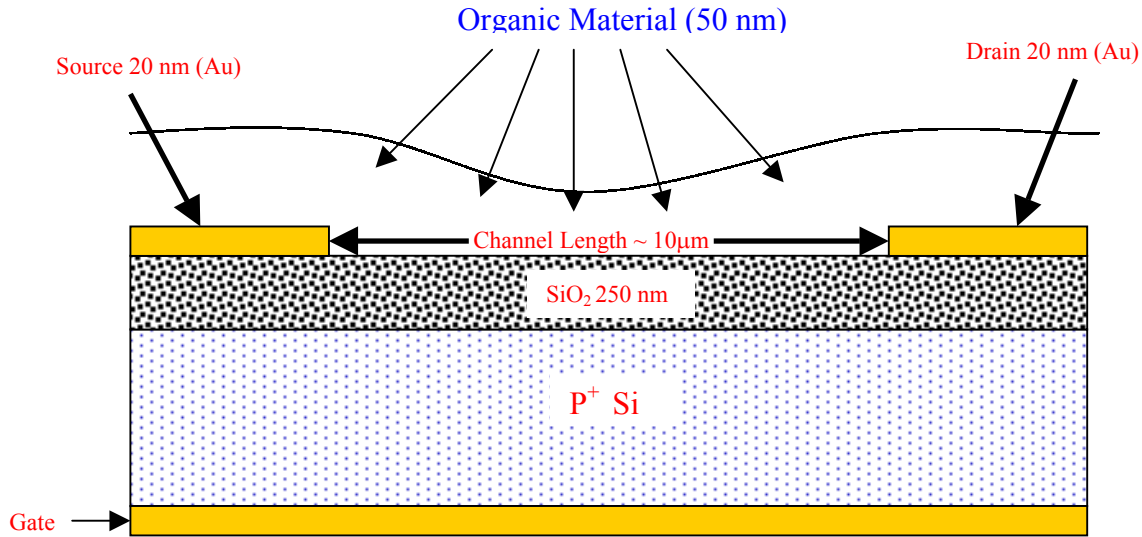


Figure 8. Illustration of the OFET devices structure developed for the Phase I project. This is the so-called bottom-contact structure in which the source and drain contacts are directly deposited on the gate oxide.

Figure 9 is a photograph of the top surface (oxide side) of the silicon wafer after this process has been completed. The source/drain contacts are clearly visible. The blue color in the photograph is due to a deposited organic layer. Individual “devices” are formed by scratching away the organic material around two adjacent contacts. One contact serves as the source and the other the drain.

The degree of coverage attained by the organic material was, at least partially, observed from a series of scanning electron microscope (SEM) micrographs. Samples were cleaved through the source/drain contacts so that the metal/organic interface would be on the edge of the samples. In Figure 10(a) the surface topography of the organic material between two adjacent contacts is shown. The organic material appears to flow over the contacts and down into a valley between them. The contact profile is reflected in the contour of the organic layer as can be readily seen in Figure 10(b). The cleaved metal surface is rather rough and a limiting factor in what can be learned from the SEM micrographs about the interface. In Figure 11 we show another closeup of the metal/organic interface with the various material layers identified. Note that there appears to be a kink in the organic layer caused by the abrupt change in the surface topology at the interface. This is an example of improvement to be made in the follow-on program. Overall the fabrication technique has resulted in successful operation of OFETs.

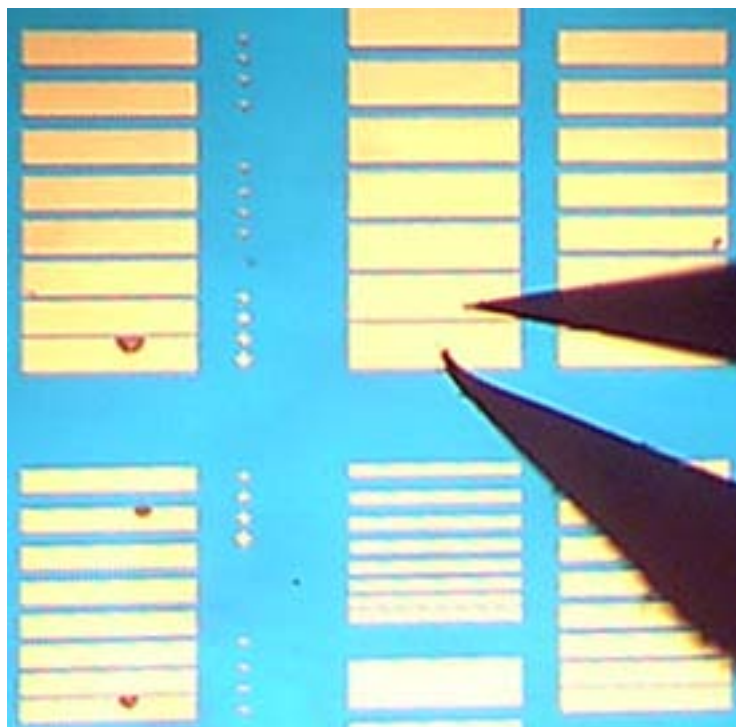
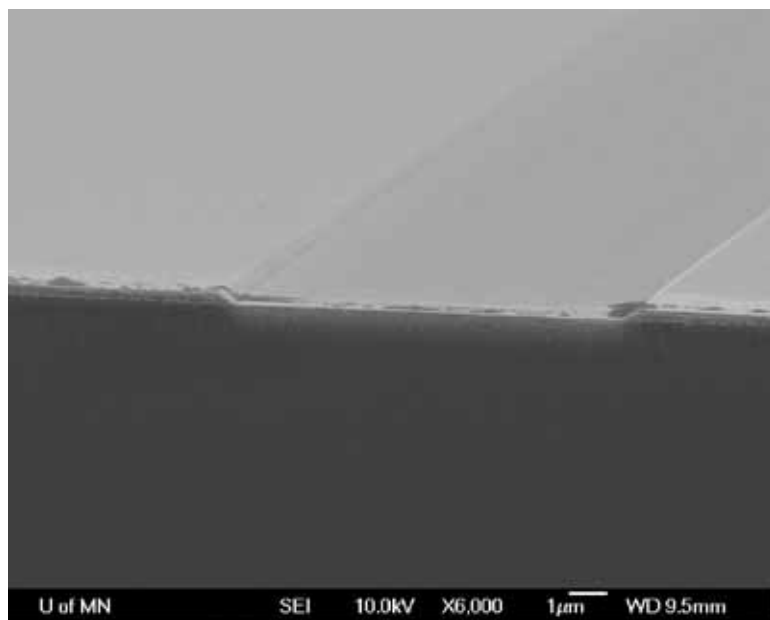
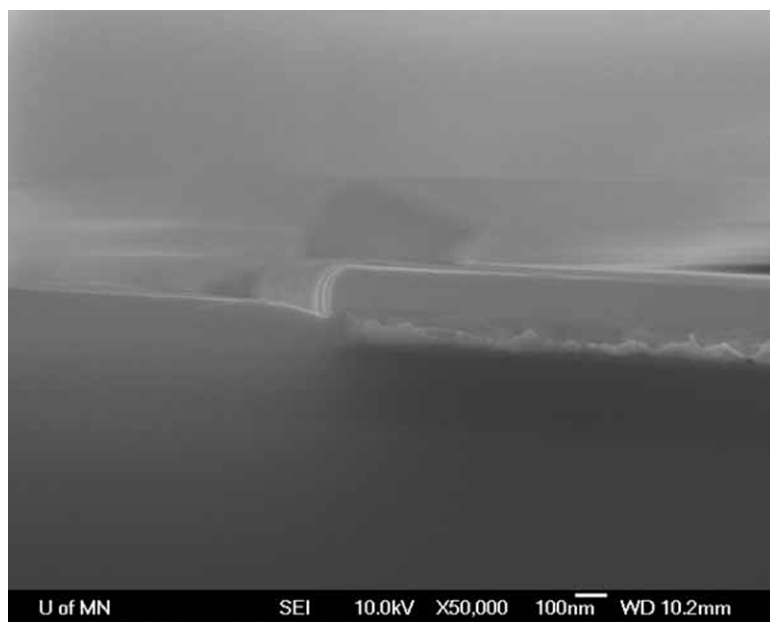


Figure 9. Photograph with microscope of drain and source contacts of the OFET structure used for this program. The blue color is due to the organic layer. Device isolation is obtained by scratching away the organic material between devices using, e.g., probe tips.



(a)



(b)

Figure 10. SEM micrographs of (a) the organic layer between two adjacent contacts and (b) in the neighborhood of a single contact.

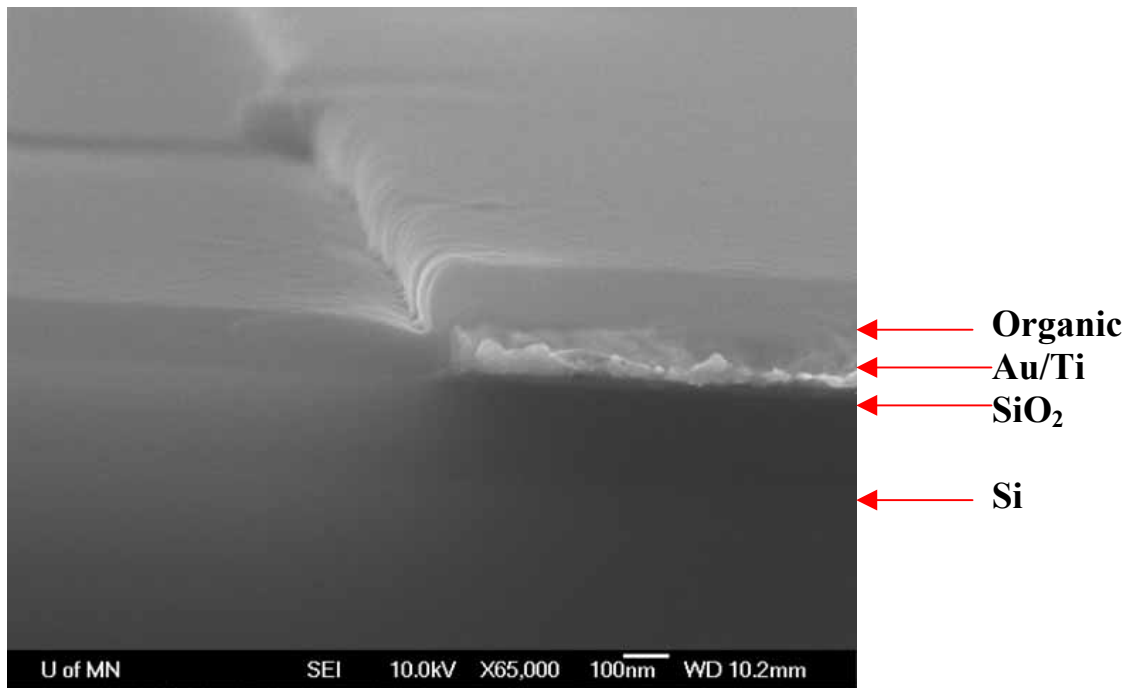


Figure 11. A SEM micrograph of the metal/organic interface similar to that of Figure 10(b) with the individual layers identified. The metal layer doesnot appear smooth because the cleaving could not produce a clean cut.

5. Material and Device Characterization

Thickness Measurement

The thickness of the organic layers are measured by using an optical interference method. This required the use of a microscope, light source, Ocean Optics spectrometer and supporting software (see Figure 12). An observed interfeference pattern like the one in Figure 13 is readily translated into a thickness value.

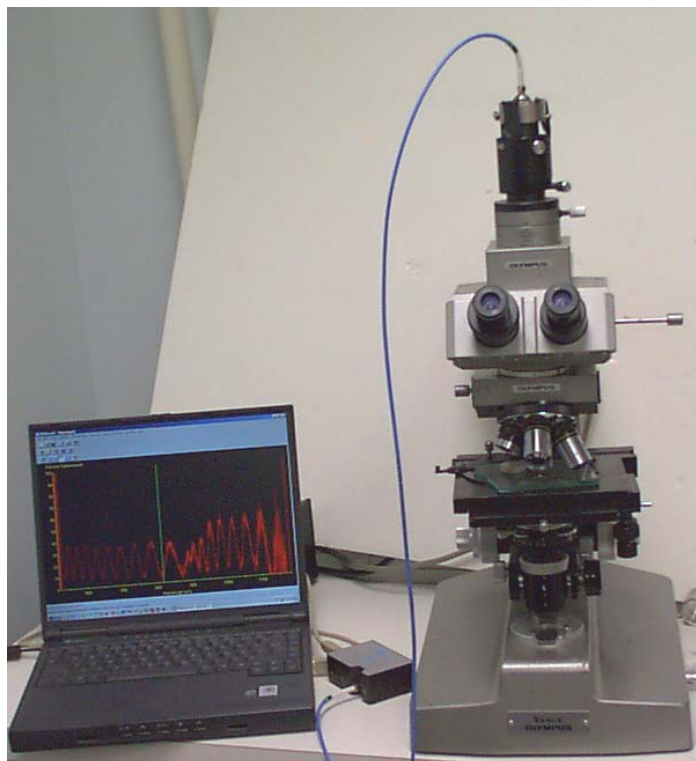


Figure 12. Optical setup for measuring thickness of organic films. It consists of a microscope, light source, Ocean Optics spectrometer and related software.

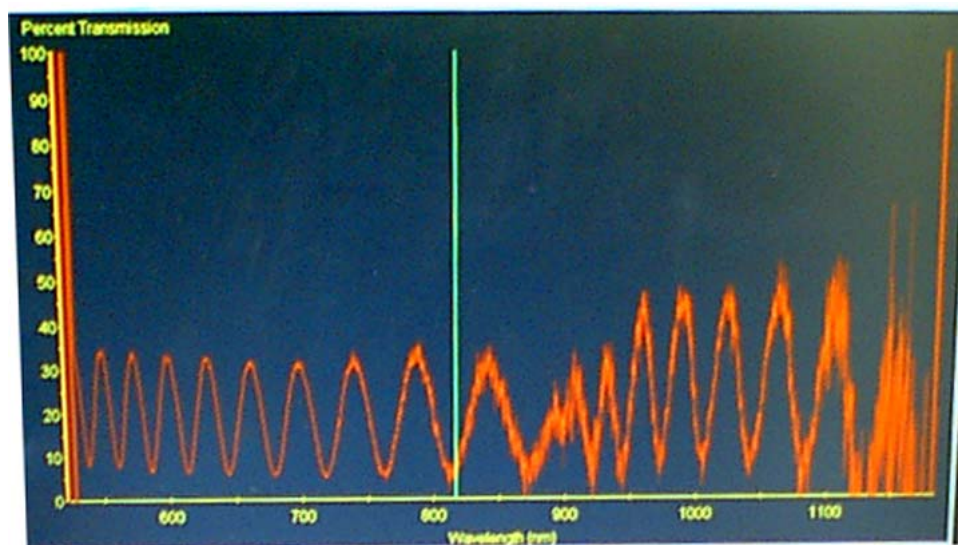


Figure 13. Interference pattern observed with the Ocean Optics spectrometer for an Alq₃ test film deposited at SVT Associates about 4 μm thick.

Electrical Characterization

The electrical measurements were made with a HP4156A parametric analyzer. The samples were left in wafer form and placed on a probe station for connection to the analyzer as shown in Figure 14. The backside gate connection is made directly to the probe station chuck. Prior to measurement device isolation was achieved by carefully scratching away the organic material around the test device with a probe tip. This proved to be a somewhat tedious task requiring practice.

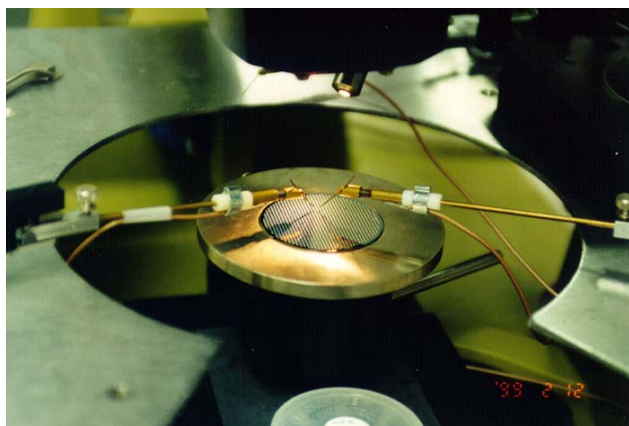


Figure 14. Photograph of a wafer on a micro-probe station used for making connections from a test device to a parametric analyzer.

Three different materials were deposited to form OFETs. For two of these materials no current was observed with the parametric analyzer when gate and drain voltages were applied. In the case of the third material, however, operating OFETs were observed. An example of the IV characteristics of a poorly or non-working device is given in Figure 15. This can be compared to the characteristics curves of working devices shown in Figures 16, 17 and 18. These represent typical results for devices with 10, 20 and 30 μm channels, respectively. The maximum currents obtained in the working devices were typically quite small, measuring in the pA range. This is not surprising since the material, NPB, has a reported mobility of about $10^{-4} \text{ cm}^2/\text{V}\cdot\text{s}$ (Forsythe et. al., J. Phys. Chem. B. 104, 3948 (2000)). NPB is also a hole transport material. Nonetheless the current modulation by the applied gate voltage is unmistakable. The measurements shown in these figures were all done in the dark, i.e., with no background light.

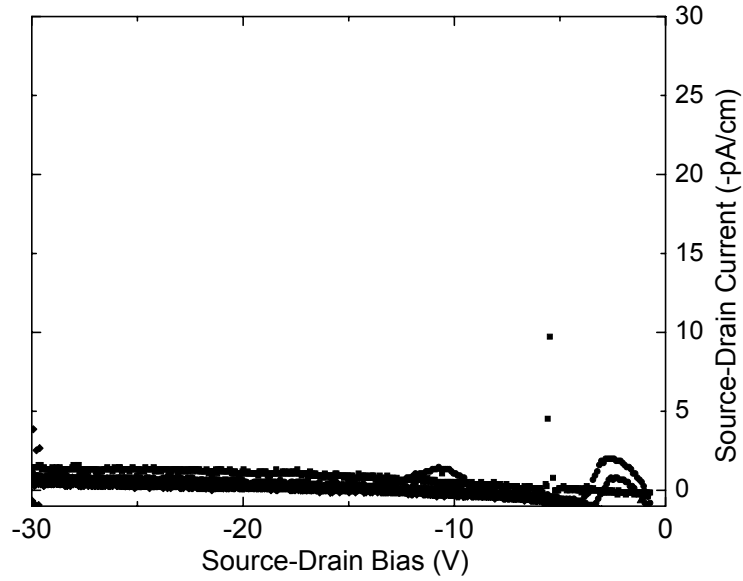


Figure 15. Characteristic IV curves for a poor 10 μm channel OFET. The gate-to-source voltages for the different curves are -5V , -10V , -15V , and -20V .

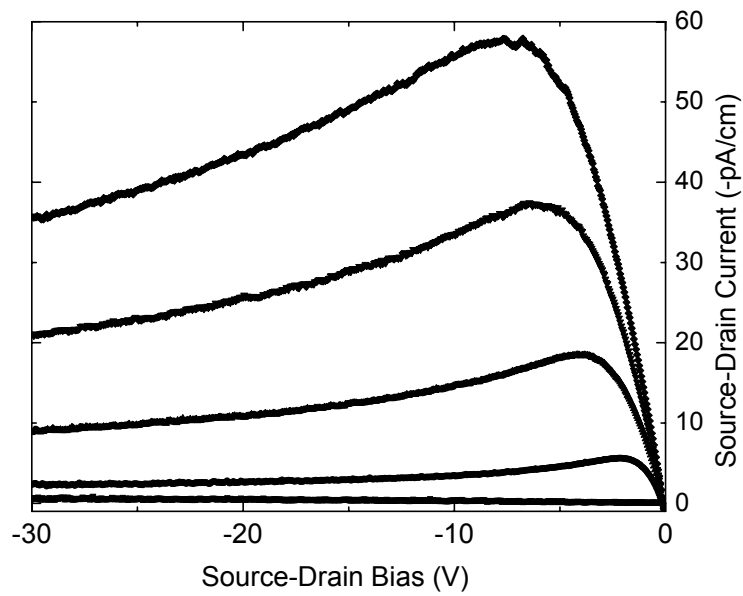


Figure 16. Characteristic curves for a 10 μm channel OFET. The gate-to-source voltages for the different curves are -5V , -10V , -15V , and -20V .

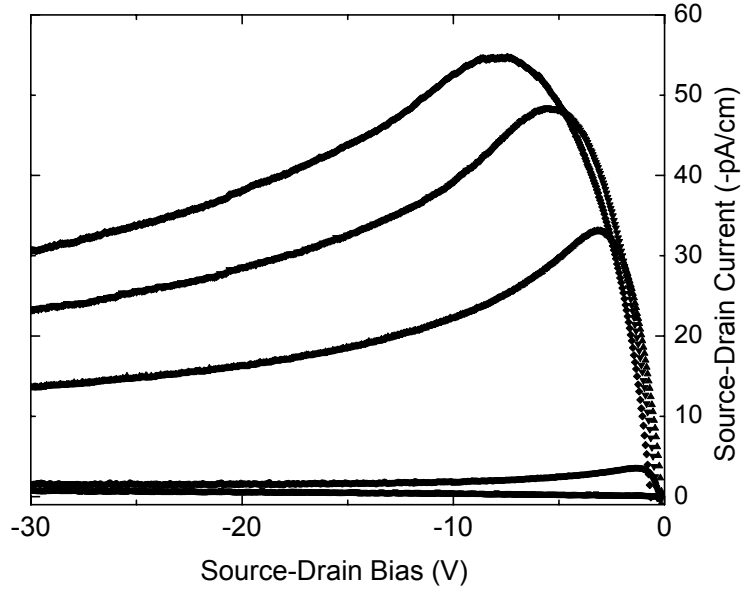


Figure 17. Characteristic curves for a 20 μm channel OFET. The gate-to-source voltages for the different curves are -5V, -10V, -15V, and -20V.

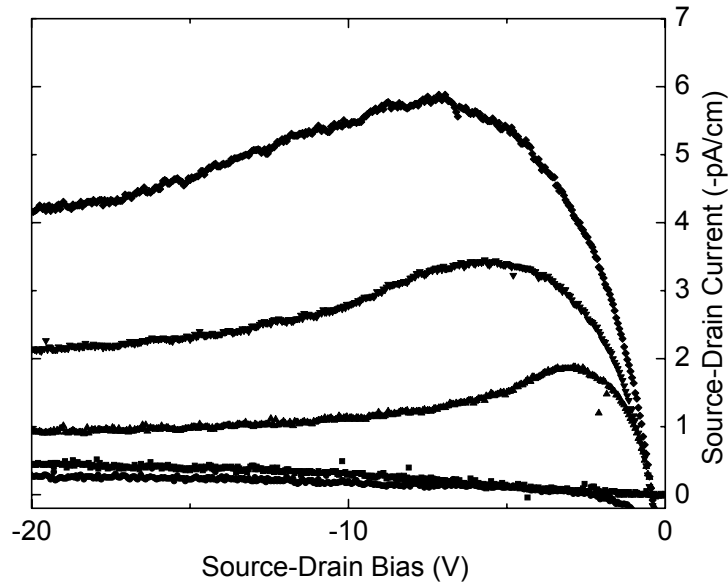


Figure 18. Characteristic curves for a 30 μm channel OFET. The gate-to-source voltages for the different curves are -5V, -10V, -15V, and -20V.

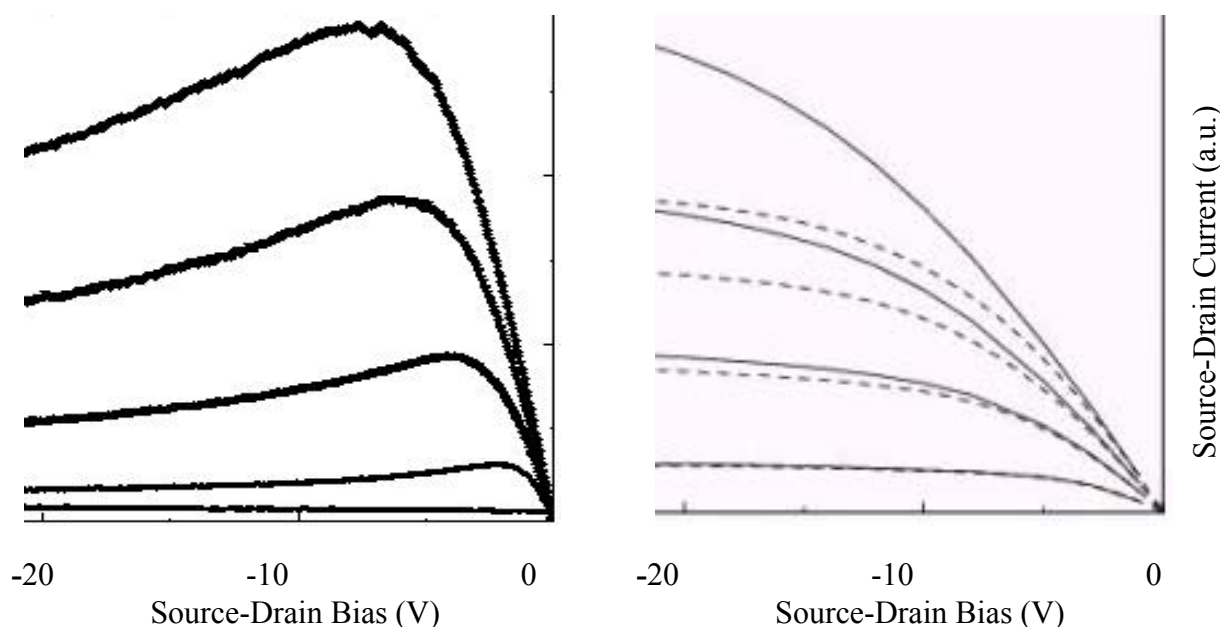


Figure 19. Side by side comparison of the IV characteristics of an OFET as determined by (a) measurement and (b) modeling. (Taken from Figures 3 and 16.)

To help make the comparison between the measured results and those predicted by the modeling easier, in Figure 19 we provide a side by side comparison between the two results. The source-drain current has been scaled. The transistor action of the device is clearly shown, and the general trend of the gate voltage modulated current is very similar to the modeling result. Given that many of the material properties are not well known, the agreement is quite striking. The device shows noticeable current slump at high applied bias voltage. This can be significantly improved with material and device optimization.

As noted above the magnitude of the saturation currents for the devices we successfully fabricated are quite small. This is in part due small mobility of the deposited organic layer. It may also be due in part the contact/organic interface. Recall that the source/drain contacts were fabricated by first depositing a thin Ti layer (~ 200 Å) prior to depositing the gold contact layer. The conducting channel (as predicted by modeling) is actually much less than this so that charge is being injected into the channel through the Ti and not the gold. The problem with this is that Ti has a smaller work function than gold and, hence, the charge injection is much less efficient for hole transport material. The Ti layer is still required for adhesion because gold does not stick well to SiO_2 . To overcome this problem we plan to recess the contacts into the SiO_2 so that the Ti layer is below the organic layer and the organic material comes into direct contact with the gold.

Since the current magnitudes involved are so small achievement of isolation becomes more difficult. Referring to Figures 16-18, the best isolation was achieved for the $10\text{ }\mu\text{m}$ channel device. For the 20 and $30\text{ }\mu\text{m}$ channel devices the IV curves show non-zero current at zero drain bias and non-zero gate bias as a consequence of incomplete isolation. Why this is so can be seen by referring to the photograph in Figure 9 where it can be seen that adjacent devices share

contacts. This creates problems when trying to isolate individual devices. The 10 μm channel devices are more isolated than the 20 or 30 μm channel devices since one of their contacts stands alone and is not shared leading to improved isolation. In the future improvement in device isolation will be achieved by redesigning the mask and the implementation of more sophisticated processing steps.

Analysis of Transistor Characteristics

Analysis of the family of I-V characteristics in Figure 20 indicates that knee voltage increases from -3V to -10V as the gate bias increases from -5V to -40V . However the current overshoot as it reaches the knee voltage decays with a comparable rate for different gate biases. The current decay follows the square root law supporting the notion that widening of the depletion layer is blocking current flow through the channel leading to current overshoot.

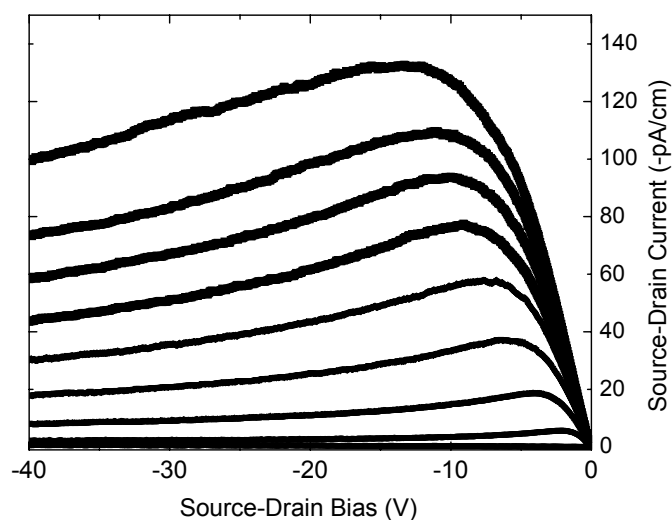


Figure 20. Source-Drain current as a function of Source-Drain Voltage for p-channel OFET device with 10 μm channel. V_g is 0V, -5V, -10V, -15V, -20V, -25V, -30V, -35V, -40V for the curves plotted from bottom to top.

Saturation current and transconductance as a function of gate voltage were obtained from the I-V characteristics plotted in Figure 20. The saturation current increases quasi-linearly with the gate bias up to maximum of gate bias applied. (see Figure 21). Figure 21 shows that there is no saturation of Source-Drain current increase when high gate biases are applied to the device. The values for transconductance of Figure 22, as derived from the data in Figure 21, are low due to low carrier concentration and mobility in the organic layer. This is in agreement with the observed response of the OFET to applied UV light as described below.

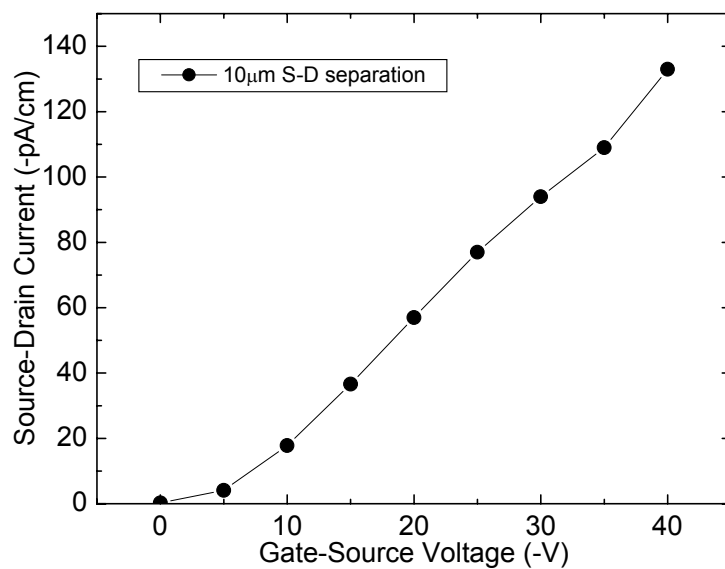


Figure 21. Saturation current for OFET device with 10μm channel.

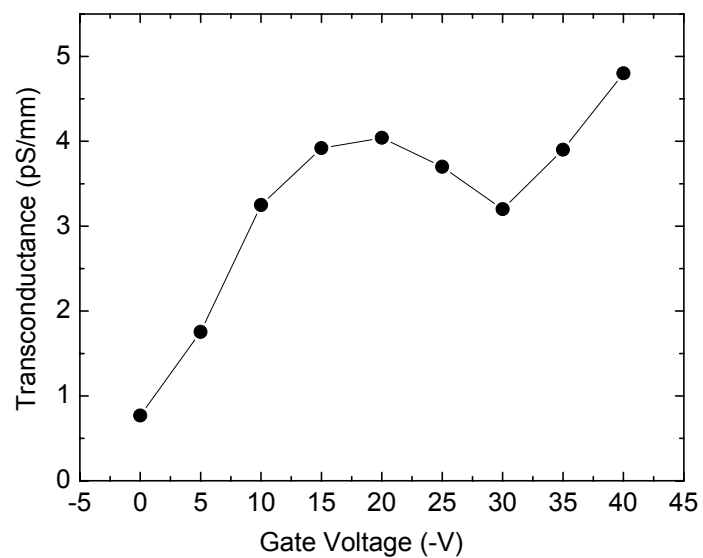


Figure 22. Measured Transconductance for OFET device with 10μm channel.

Organic field effect transistors show promise for a variety of applications. These include low-cost electronics, displays, RF ID tags, and sensors. Some of these applications will be the focus of the follow-on program. Here, as shown in Figure 23 organic materials may be highly sensitive to UV light. Under exposure to UV at 300 nm the saturation current increases by ~ 2 orders of magnitude as can be seen by comparing Figure 23 to Figure 17. Note too that a drop in current with increasing drain voltage is not apparent suggesting that the UV light generates enough carriers to overcome this effect.

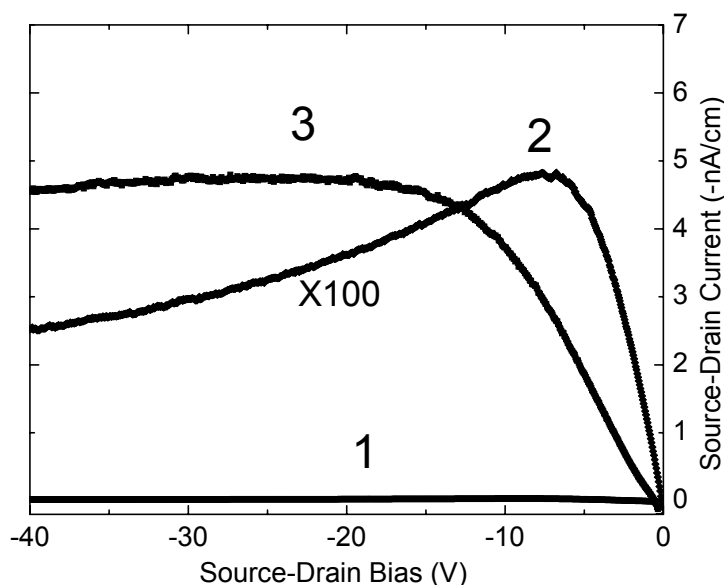


Figure 23. Comparison between Source-Drain bias vs. Source-Drain current curves for (1) a 20 μm channel OFET in the dark, (2) a 20 μm channel OFET in the dark with current multiplied by 100, and (3) exposed to 300 nm UV light. The gate-to-source voltage is -20 V in all three cases.

6. Summary of Conclusions

The Phase I effort emphasized modeling for optimization of device performance and the fabrication of bottom-contact organic-based FETs. The modeling results revealed the strong influence that the nature of the contact/organic interface has on overall device performance. The presence of voids or other defects can greatly degrade the quality of the device. To meet the goals of the program a simple mask was used for defining the source/drain contacts. Significantly, working OFETs with 10, 20 and 30 μm channels were demonstrated. These results set the stage for continuing improvement in OFET performance and their utilization for various applications to be pursued in the follow-on phase of the program.

Future work includes further development of the modeling to optimize device design and achieve improved performance. The growth of the organic material needs to be optimized further to improve OFET performance. Special attention will be paid to gain higher carrier concentration in the organic layers through development of the intentional doping and co-doping process that will enable higher current handling capabilities of the devices. Novel device designs such as modulation doped transistor structures will be explored in the Phase II program. In the new transistor design we will test a concept of separating the carrier generation layer from the carrier transport layer with modulation doped organic heterostructures.

In addition, more sophisticated masks and processing techniques shall be developed to improve isolation and address applications such as chemical sensing, RF identification and display drivers.